AMENDMENTS TO THE SPECIFICATION

Please delete paragraph [01] and replace it with the following amended paragraph:

[01] ~~[Not Applicable]~~ The present application is a continuation of U.S. Application Serial No. 10/100,757 filed March 19, 2002, which is a continuation-in-part of U.S. Application Serial No. 09/775,701 filed February 2, 2001, now U.S. Patent No. 6,411,557 issued June 25, 2002, the complete subject matter of each of which is incorporated herein by reference in their entirety.

Please delete the Abstract of the Disclosure and replace it with the following amended Abstract of the Disclosure:

The present invention relates to a synchronous self timed memory device. The device includes a plurality of memory cells forming a cell array, at least one local decoder interfacing with the cell array, at least one local sense amplifier and at least one local controller. The local sense amplifier interfaces with at least the decoder and cell array, and is adapted to precharge and equalize at least one line coupled thereto. The local controller interfaces with and coordinates the activities of at least the local decoder and sense amplifier. One embodiment of the present invention relates to a memory device comprising a plurality of synchronous controlled global elements and a plurality of self-timed local elements. In this embodiment, at least one of the solf-timed controlled local elements interfaces with the synchronous controlled global element.